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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,053	04/21/2004	Sanjeev Aggarwal	TI 35817	6820

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EXAMINER	
CHAUDHARI, CHANDRA P	
ART UNIT	**PAPER NUMBER**
2891	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,053	AGGARWAL ET AL.	
	Examiner	Art Unit	
	Chandra Chaudhari	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-13,17-21,23-30 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-13,17-21,23-30 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 5, 7-13, 17-18, 21, 23-30, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata – US 6,232,174 and Grieger – US 5,855,811.

Nagata (Figs. 2A-2F and text in col. 4, lines 2-64, and col. 8, line 41 to col. 9, line 62) discloses substantially the claimed invention by manufacturing a ferroelectric random access memory with a transistor having source/drain regions 4, interlevel dielectric layer 5 with conductive plug 6, forming 1st electrode 7, forming 2nd electrode 11 over the planarized ferroelectric dielectric layer 8. Nagata does not disclose to clean the planarized ferroelectric dielectric layer, nor planarizing and cleaning the electrodes. Greiger (abstract, and col. 1, lines 13-41, and col. 2, lines 13-65) teaches to planarize layers and clean during semiconductor fabrication.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to planarize and clean each layer as taught by Grieger in Nagata's process to build up uniform layers which economizes on process time and cost and clean the planarization residue from the surface to efficiently make contact with subsequent layers.

Claims 3-4, 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata and Grieger as applied to claims 1-2, 5, 7-13, 17-18, 21, 23-30, 32 above, and further in view of either (Suenaga - US 6,239,457 or Suh - US 6,338,970).

Nagata and Grieger are applied as above and do not disclose the ferroelectric dielectric layer having an average surface roughness of less than about 0.5 nm. Either (Suenaga (Fig. 7A and col. 7, lines 1-49) or Suh (Fig. 2A-2C and col.2, line 49 to col. 3, line 37)) teaches to form a ferroelectric dielectric layer with an average surface roughness of less than about 0.5 nm.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a ferroelectric dielectric layer with an average surface roughness of less than about 0.5 nm as taught by either (Suenaga or Suh) in (Nagata and Grieger's process) to decrease leakage current and increase breakdown voltage.

Claims 1-2, 5, 7, 12-13, 17-18, 21, 23, 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata - US 6,232,174 and Lee - US 2002/0003123.

Nagata (Figs. 2A-2F and text in col. 4, lines 2-64, and col. 8, line 41 to col. 9, line 62) discloses substantially the claimed invention by manufacturing a ferroelectric random access memory with a transistor having source/drain regions 4, interlevel dielectric layer 5 with conductive plug 6, forming 1st electrode 7, forming 2nd electrode 11 over the planarized ferroelectric dielectric layer 8. Nagata does not disclose to clean the ferroelectric dielectric layer. Lee (Fig. 1 and paragraphs 38-41) teaches to clean the ferroelectric dielectric layer prior to forming the 2nd electrode layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to clean the ferroelectric dielectric layer as taught by Lee in Nagata's process to remove damaged portions, thereby reducing leakage current.

Claims 3-4, 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata and Lee as applied to claims 1-2, 5, 7, 12-13, 17-18, 21, 23, 28-30 above, and further in view of either (Suenaga - US 6,239,457 or Suh - US 6,338,970).

Nagata and Lee are applied as above and do not disclose the ferroelectric dielectric layer having an average surface roughness of less than about 0.5 nm. Either (Suenaga (Fig. 7A and col. 7, lines 1-49) or Suh (Fig. 2A-2C and col.2, line 49 to col. 3, line 37)) teaches to form a ferroelectric dielectric layer with an average surface roughness of less than about 0.5 nm.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a ferroelectric dielectric layer with an average surface roughness of less than about 0.5 nm as taught by either (Suenaga or Suh) in (Nagata and Lee's process) to decrease leakage current and increase breakdown voltage.

Applicant's arguments with respect to claims 1-5, 7-13, 17-21, 23-30, and 32 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chandra Chaudhari whose telephone number is 571-272-1688. The examiner can normally be reached on Mon - Fri (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chandra Chaudhari
Primary Examiner
Art Unit 2891

C. Chaudhari
Chandra Chaudhari
March 3, 2006